One-Chip GaAs Monolithic Frequency Converter Operable to 4 GHz

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Abstract—**A GaAs monolithic frequency converter integrated circuit that operates at frequencies up to 4 GHz has been developed. It combines a feedback amplifier, a differential amplifier, a double-balanced mixer, a voltage-controlled oscillator, and an IF amplifier on a 1-mm^2 GaAs chip. The FET circuits were matched by digital IC design rather than by the distributed element network technique, to use the substrate more effectively. Self-aligned WSi/Au gates 1.5 μm long were used, and the resistance in conventional WSi gates was reduced to enhance microwave characteristics. At 4 GHz, the conversion gain is 18 dB, the DSB noise is 11.8 dB, and the output power is 5.6 dBm.**

I. INTRODUCTION

ANTICIPATING that GaAs integrated circuits (IC's) will be used in ultra-high-speed computer and microwave communication systems, various applicable circuits have been studied [1], [2]. For microwave communication systems, GaAs monolithic IC's are especially effective in high-frequency applications such as RF front ends. Amplifiers, frequency dividers, mixers, and other basic circuits have been developed to produce these IC's. Recently, circuits that combine these functions have also been studied [3], [4].

This paper presents a prototype IC which integrates a feedback amplifier, a differential amplifier, a double-balanced mixer, a voltage-controlled oscillator, and an IF amplifier on a 1-mm^2 chip. We used digital IC technology instead of FET matching to make more efficient use of the substrate. The outputs of the voltage-controlled oscillator are 180° out of phase. These outputs are suitable for supplying the clock and the inverted clock for a frequency divider used in a phase-locked oscillator. These circuits were designed using SPICE.

Conventionally, the WSi self-alignment gate process is used to manufacture IC's, but the high resistance of WSi has made the microwave characteristics inadequate. In our prototype, Au was deposited on the WSi to reduce gate resistance. The maximum available power gain was improved in our FET's, with less noise in the amplifiers [5]. For frequency converter IC's, a conversion gain of 18 dB was obtained at an input of 4 GHz.

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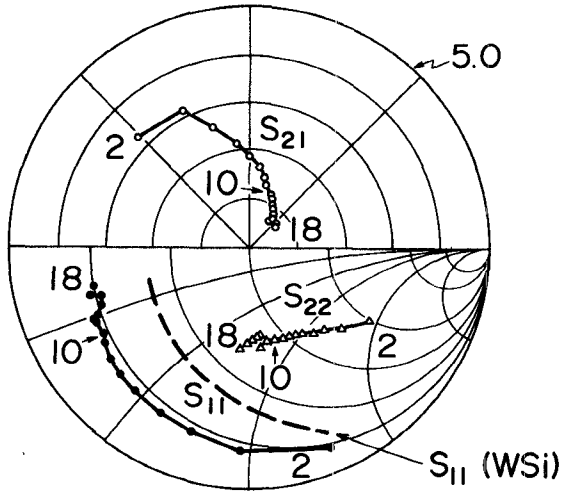

Fig. 1. FET S parameter (gate width, 400 μm; gate length, 1.5 μm). The dashed line indicates S_{11} for a WSi gate FET with the same dimension.

II. UNIT CHARACTERISTICS

WSi self-aligned gate process technology has proven useful in producing IC's, especially LSI circuits, and is suitable for uniform production of FET's. In microwave circuits, where unit performance is important, however, this process is sometimes inadequate because of the high resistance of WSi. We used a WSi/Au gate composition to reduce the gate resistance. The resistivity decreased from 2×10^{-4} Ω·cm to 1.3×10^{-5} Ω·cm, and microwave characteristics were greatly improved.

Fig. 1 shows the S parameters of the prototype FET. The FET's gate width was 400 μm and the gate length 1.5 μm. A pinch-off voltage of −0.8 V and a transfer conductance of 125 mS/mm ($V_{gs} \doteq 0$ V) were obtained. For the WSi gate FET's, S_{11} lies near the center of the Smith chart, but our FET's were placed on a resistance line (about 10 Ω) and there was little gate resistance effect.

The maximum available power gain is shown in Fig. 2. With the WSi gate, the gain was 1 dB at 12 GHz, and with the WSi/Au gate, it increased to 4 dB. FET's having a gate length of 1 μm provide a maximum available power gain of 8.5 dB, and the characteristics approach those of other FET's having equivalent gate lengths. We found that IC's produced by the WSi/Au self-alignment process are suitable for microwave applications.

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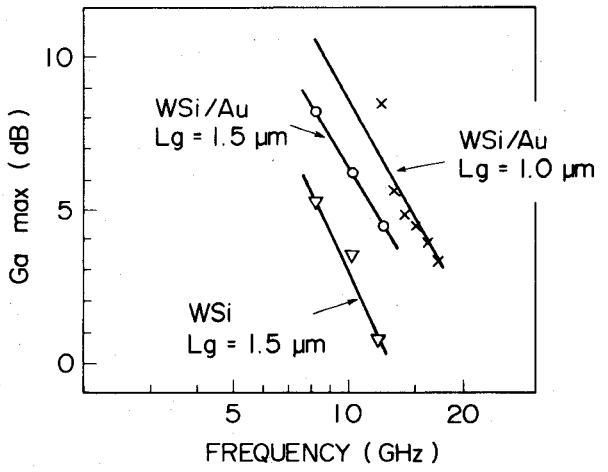

Fig. 2. Ga(max) of the FET (gate width, 400 μm; gate lengths, 1.5 μm and 1.0 μm).

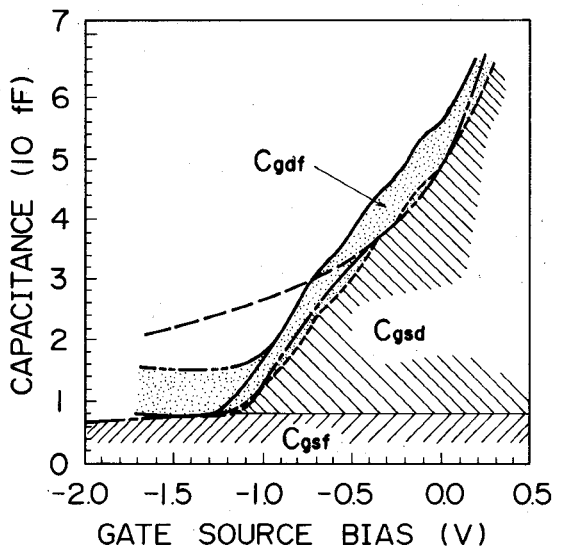

Fig. 3. FET capacity (gate width, 20 μm; gate length, 1.5 μm) for gate–source voltage. Solid line: measured capacitance between the gate terminal and source terminal when the source and drain are not strapped. Two-dots-dash line: measured capacitance between the gate terminal and the source terminal when source and drain are strapped. Dotted line: gate–source capacitance (target value for fitting) from which the drain–source capacitance is subtracted. Dashed line: curve proportional to $-1/2$ power of gate–source voltage. Dot-dash line: curve modeled as the gate–source capacitance.

III. FET Model

To simulate each circuit, prototype FET's were evaluated and the parameters of the equivalent circuit were determined. SPICE was used as the circuit computation program. Great care was taken with the capacitance model. Details are given in Fig. 3. The solid line is the measured capacitance value between the gate terminal and the source one when source and drain are separated (FET connection), and the two-dots-dash lines the capacitance value when source and drain are strapped (diode connection). Where the FET is not pinched off, the capacitance values are equal. This is because source and drain terminal is connected in the FET channel region. For both cases, we measured the total value for the fringing capacitance (C_{gsf}),

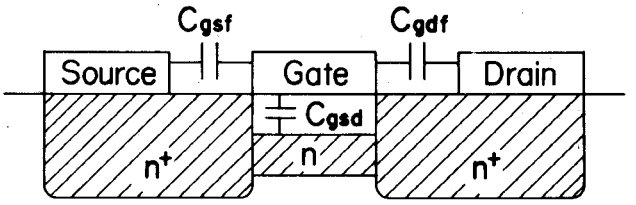

Fig. 4. FET capacitance model.

the depletion region capacitance (C_{gsd}), and the gate–drain fringing capacitance (C_{gdf}) shown in Fig. 4. When the FET is pinched off by the deep gate voltage, C_{gsd} becomes negligible. Thus, for the FET connection, the measured capacitance equals that for C_{gsf}. The measured value changes greatly at the threshold voltage. For the diode connection, the measured capacitance equals the total value for C_{gsf} plus C_{gdf}, indicating that the value did not change as much. The capacitance regions are showed in Fig. 3. We consider C_{gs} in the FET model to equal the total value of C_{gsd} plus C_{gsf}, and C_{gd} to equal C_{gdf}.

For the self-aligned gate FET, the gate is very close to the n^+ region, and the depletion region does not expand to the n^+ region when a bias voltage is applied to the drain–source terminal. The depletion region is thin enough compared with the gate length, and the effect of the bias on the capacitance at the gate–drain edge or the gate–source edge is small. We therefore assume C_{gsf} and C_{gdf} to be constant for the FET model. These values agreed well with the capacitance values calculated by the S parameters. Therefore, the value of the dotted line in Fig. 3 is C_{gs}.

It is generally accepted that capacitance changes inversely to the square root of the gate voltage [6]. This model is based on the assumption of uniform donor density distribution in the active layer. There was, however, a large shift around the threshold value, as show by the dashed line in Fig. 3. To obtain results near the measured values, we used linear compensation between the portion where values change as the square root of the bias and the section of the gate source voltage lower than the threshold value. This modeled curve (dot–dash line in Fig. 3) is very close to the target carve (dotted line). The fundamental equations are

$V_{gs} < V_1$

$$C_{gs} = A \cdot \epsilon \cdot \tan^{-1} \sqrt{\frac{V_{bi} - V_{th}}{V_{th} - V_{gs}}} \tag{1a}$$

$V_1 < V_{gs} < V_2$

$$C_{gs} = B \cdot V_{gs} + C \tag{1b}$$

$V_{gs} > V_2$

$$C_{gs} = D \cdot \left(\frac{V_{bi} - V_{th}}{V_{bi} - V_{gs}} \right)^x \tag{1c}$$

where V_1 and V_2 are the gate–source bias voltages, determined by optimization; V_{th} is threshold voltage (V_{th} is between V_1 and V_2); V_{bi} is the built-in voltage; ϵ is the

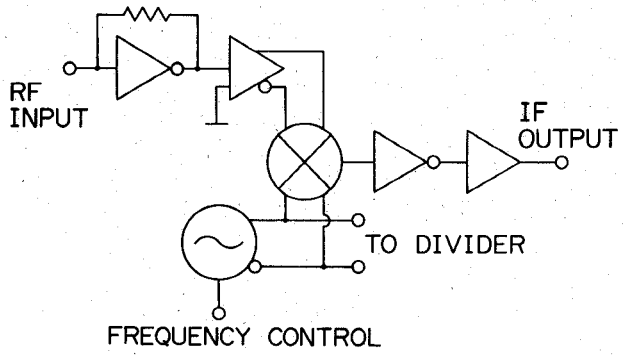

Fig. 5. Block diagram of frequency converter.

dielectric constant; and A, B, C, D, and X are the constant coefficients determined by optimization.

IV. Circuit Configuration

A block diagram of the frequency converter circuit is shown in Fig. 5. The frequency converter circuit amplifies the RF input and generates positive and opposite phases using the feedback and differential amplifiers. The local frequency from the astable multivibrator is input to the double-balanced mixer and the frequency divider (another IC). The IF amplifier is a one-stage high-gain amplifier.

Fig. 6 shows a schematic diagram of the frequency converter. The feedback amplifier uses buffers for the feedback loop. In a conventional feedback amplifier with a direct connection, feedback is provided directly via a resistor from the level shift circuit. High impedance is desirable at the output of the level shift circuit. The input side impedance observed from the level shift circuit is several hundred Ω, lower than the FET's input impedance. To handle this, we added a buffer to the feedback section to increase the impedance with respect to point A [7]. This buffer reduced the load at the level shift output and improved gain. If we adjust the circuit coefficients to obtain the same gain as the conventional type, characteristics at high frequencies improve and the bandwidth is extended. The feedback buffer also improves the isolation in the opposite direction. The feedback amplifier has an input inverter with a gate width of 200 μm, a 250 Ω resistor (B), a level shifter, and a feedback buffer with a gate width of 40 μm and feedback resistance of 150 Ω.

The differential amplifier has a gate width of 40 μm and a load resistance of 2 kΩ. The double-balanced mixer (AND–NOR circuit) has a gate width of 40 μm, and uses an active resistor with a gate width of 40 μm and a 1.5 kΩ passive resistor in parallel as the load.

The voltage-controlled oscillator was connected to the double-balanced mixer and the frequency divider (used as a phase-locked oscillator). Since 180°-out-of-phase outputs are desired, we used an astable multivibrator type oscillator [8]–[11]. This oscillates when the impedance at point C in Fig. 6 indicates a negative resistance. Since negative resistance can be realized across a wide range, oscillation at any frequency below the oscillation limit can be achieved by changing the resonance conditions between the diode

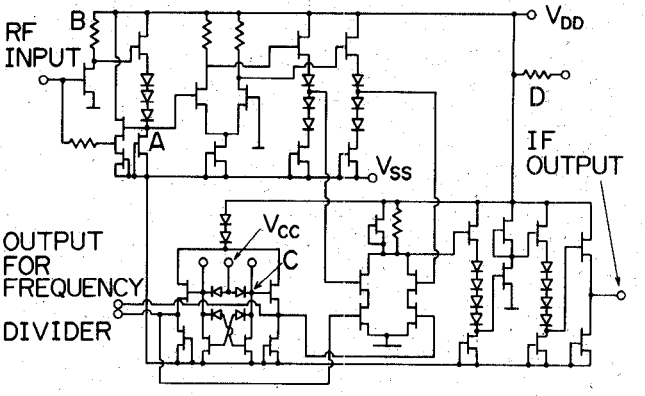

Fig. 6. Circuit configuration of frequency converter.

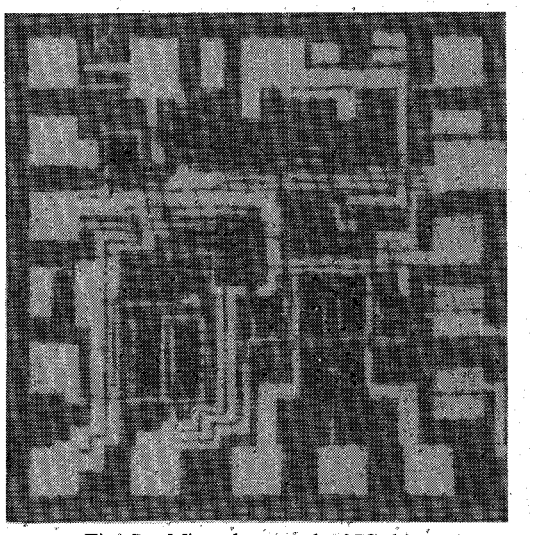

Fig. 7. Microphotograph of IC chip.

capacitance and the inductance of the outer inductor. In a WSi gate, the oscillation limit is 17 GHz [8]. In a WSi/Au gate, however, oscillation is possible at 20 GHz or higher. This oscillator had a gate width of 80 μm, and the diodes a gate length of 4 μm and gate width of 200 μm. The IF section uses a gate width of 200 μm, except for the output buffer (400 μm). The active load of the highest gain was used as an amplifier.

Two types of power supply, positive and negative, were used. The positive side is affected by interference from circuits, and resonance may occur within the band. To avoid this, we added a 50 Ω antiresonance resistor, D (Fig. 6).

V. Circuit Characteristics

Fig. 7 shows the prototype frequency converter chip. The RF section is separated by a ground strip. A 0.5-mm-wide line on a ceramic board was used as the oscillator inductor. The frequency converter circuit operates on a supply voltage of ±5.5 V or higher, with a current consumption of about 60 mA.

The conversion gains were 32 dB for 1 GHz, 28 dB for 2.35 GHz, 21 dB for 3.9 GHz, and 18 dB for 4.16 GHz, with an IF of 70 MHz as shown in Fig. 8. These character-

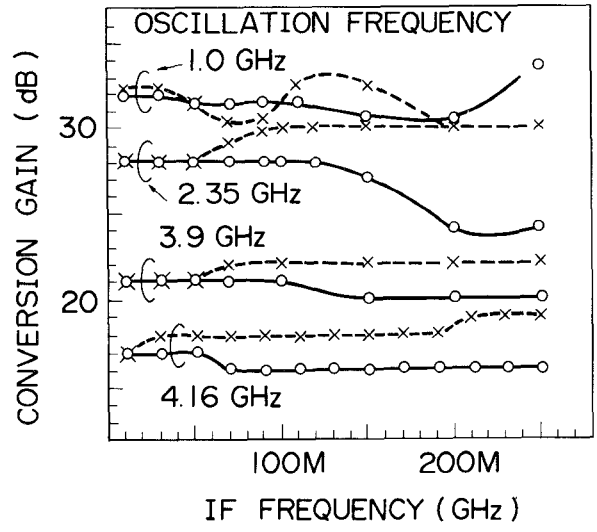

Fig. 8. Conversion gains of frequency converter. Solid line: input frequency higher than the oscillation frequency. Dashed line: input frequency lower than the oscillation frequency.

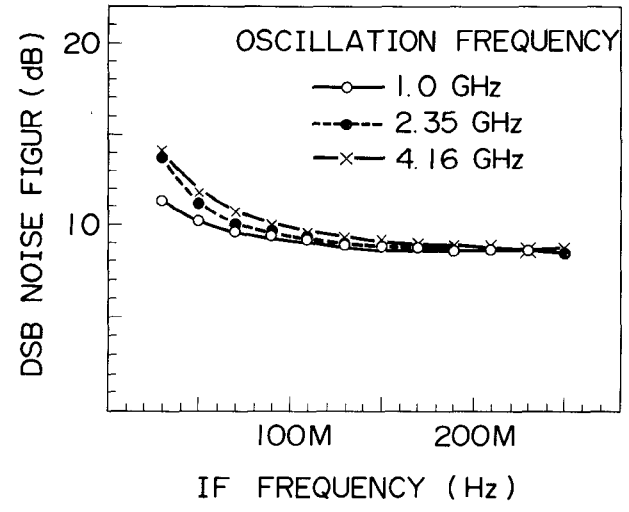

Fig. 10. DSB noise figure of frequency converter.

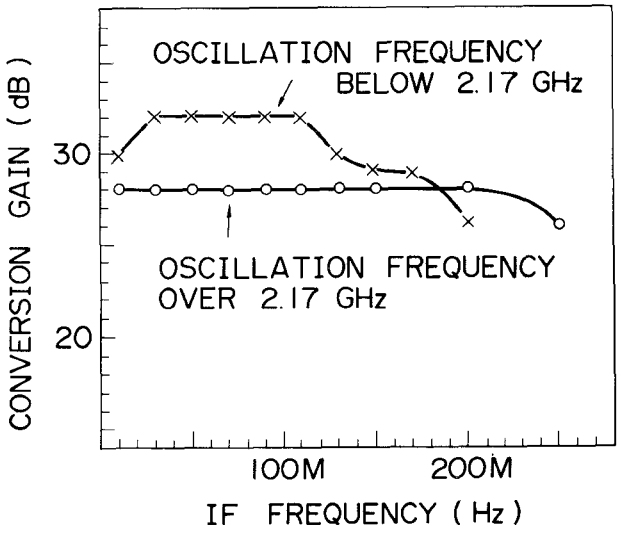

Fig. 9. Conversion gains of frequency converter.

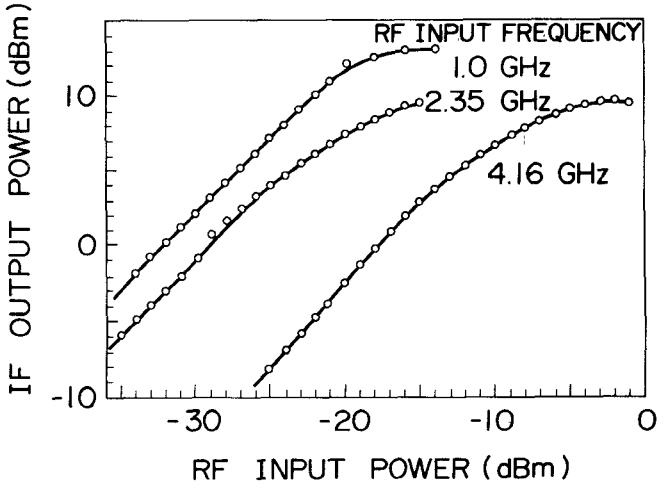

Fig. 11. Input and output characteristics of frequency converter.

istics were obtained when the input RF was changed, keeping the oscillation frequency constant. When the frequency of the oscillator was varied and the input RF was fixed at 2.17 GHz, a conversion gain between 28 and 32 dB was obtained. Fig. 9 shows these characteristics. The gain varies at a control voltage of -1 V or less. When it exceeds -1 V, the gain is constant.

When the IF decreases, the DSB noise increases as shown in Fig. 10. This is probably because noise near the oscillation frequency and the $1/f$ noise of the IF amplifier increase. The results obtained at an IF of 70 MHz were 10.5 dB at 1 GHz, 11 dB at 2.35 GHz, and 11.8 dB at 4.0 GHz. The noise figure could be further reduced by improving the conversion efficiency of the double-balanced mixer.

Fig. 11 shows the input–output characteristics for a 70 MHz IF. The output power obtained at a gain compres-

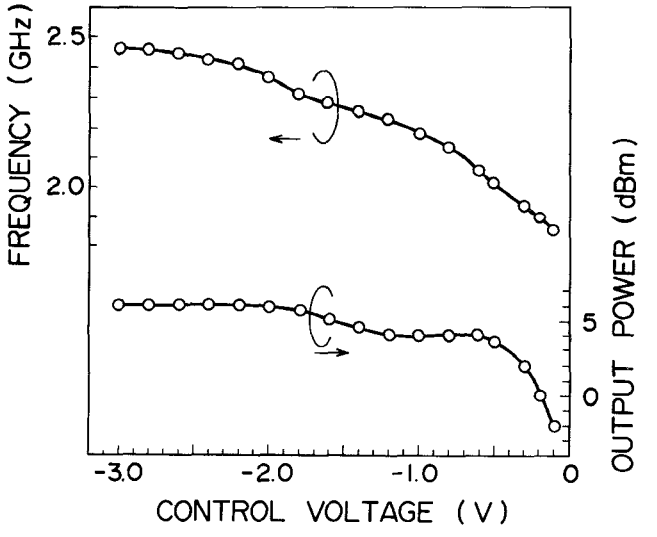

Fig. 12. Oscillation characteristics of the oscillator in the frequency converter with the stripline resonator.

sion of 1 dB was 12 dBm at 1.0 GHz, 6 dBm at 2.35 GHz, and 5.2 dBm at 4.16 GHz.

The oscillator output for the frequency divider differs with the control voltage; it is 0 to +6 dBm up to 4 GHz. The greater the bias, the greater the output value. If −1 V is exceeded, however, the output value is almost the same, and is enough to drive the frequency divider. The output characteristics at 2 GHz are shown in Fig. 12. The return loss at the RF input section was constant (about 10 dB) up to 10 GHz. The return loss at the IF output section was 13 dB or higher up to 10 GHz.

Since the oscillator can operate at up to 20 GHz, a frequency converter with higher frequency can be designed into the high-frequency amplifier part. Although production of high-frequency amplifiers over 10 GHz has been difficult, they may now be designed with the WSi/Au gate used in our prototype. We expect to attain a higher frequency front end in the future.

VI. Summary

A frequency converter IC containing an amplifier, a double-balanced mixer, an IF amplifier, and an oscillator as functional elements has been developed. The chip size is 1 mm^2. Direct-type circuits were used instead of distributed element matching networks or capacitors. Using the WSi/Au self-alignment process to enhance FET performance, we produced a compact front-end IC able to operate up to 4 GHz. The conversion gain was 32 dB for 1 GHz and 18 dB for 4 GHz, and the DSB noise was 10.5 dB and 11.8 dB, respectively. As for feasibility, the one-chip frequency converter for up to 4 GHz demonstrated the effectiveness of WSi/Au gates. Our next step is to design high-frequency and low-power-consumption frequency converters.

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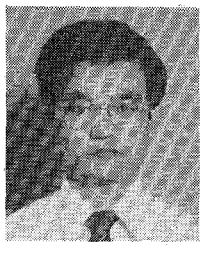

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